Low Cost, Room Temperature Debondable Spin on Temporary Bonding Solution: A Key Enabler for 2.5D/3D IC Packaging

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Abstract

We report the development of a bi-layer spin on temporary bonding solution (TBS) which eliminates the need for specialized equipment for wafer pretreatment to enable bonding or wafer post treatment for debonding. Thus it greatly increases the throughput of the temporary bonding/debonding process. It also provides a total thickness variation (TTV) of less than 1 µm for spin coated films on both 200 mm and 300 mm wafers which enable the TTV of 300 mm bonded pairs to be 2 – 3 µm for bumped wafers using 70 and 100 µm thick adhesive films after backgrinding for an unoptimized bonding process. Additionally, the time taken for the entire spin coat-bond-debond process was less than 15 minutes with room for further improvement. Based on the current results, it is expected that the current bi-layer based temporary bonding solution has the potential to play an important role in enabling the high volume manufacturing of 2.5D/3D IC stacking.

Introduction

3D IC integration has been viewed as one of the key enablers for reducing form factor while improving the electrical and thermal performance of microelectronic devices to meet the seamless needs of next generation communication devices. One of the key enablers for realizing true 3D IC integration is the ability to handle ultra thin wafers with the aid of a temporary bonded carrier support system using temporary bonding adhesives. The primary focus of this paper is to introduce a complete material solution which not only takes advantage of the inherent properties of silicones such as thermal and chemical stability but is also geared towards providing a process which is fast, simple and cost effective.

Electronic packaging in 2.5D/3D IC integration has increasingly moved from fundamental research to development and is currently marching toward high volume manufacturing. As the semiconductor industry makes this transition, one of the key hurdles in the adoption of the technology has been due to the lack of a high performance temporary bonding solution for enabling thin wafer handling. Temporary bonding solutions play the vital role of enabling the handling of thin wafers by bonding the active device wafer to a carrier wafer for subsequent wafer thinning and TSV formation. The success of the 2.5D/3D stacking technology depends on achieving a uniform coating of the temporary bonding adhesive and the bonded wafer pair being able to withstand the mechanical, thermal and chemical processes which are part of the subsequent TSV fabrication and the ability to debond the bonded wafer pair without damaging the device wafer while providing a low total cost of ownership to the end user.

Background

Wafer bonding is a technology which has been used extensively in the MEMS industry as a key enabler for constructing complicated architectures and novel applications [1-2]. Depending on the process requirements and applications wafer bonding can be classified into various groups such as direct bonding, anodic bonding, thermo-compression bonding adhesive bonding etc. [3]. The most conspicuous enabler for 3D IC integration for ultra thin wafer with Thru-Silicon-Via (TSV) technology is the use of polymer based temporary bonding adhesives and a carrier wafer as a support system for handling ultrathin device wafers [3, 4]. The primary requirements for wafer handling in the scheme of 3D integration is for the ultrathin (total wafer thickness <= 50 µm) device wafers to be protected as it moves through the various processing steps such as wafer thinning, TSV, Redistribution Layer (RDL) fabrication etc. where the ultrathin silicon wafer would bow and crack if not supported by a carrier wafer. The typical process steps established for the wafer support process for 3D integration are

a. Temporary bonding adhesive coating on device wafer,
b. Bonding of device wafer to carrier wafer
c. Wafer thinning to achieve ultrathin device wafers
d. TSV reveal, RDL and wafer interconnect fabrication
e. Debonding of processed ultrathin device wafers
f. Device wafer cleaning
g. 3D stacking of thinned device wafers.

Thus the polymer adhesive employed during the temporary bonding debonding process in 3D IC integration has to [5]

1. Protect the device wafer during the above outlined processing steps
2. Have excellent thermal and chemical stability to withstand the plasma processes as well as the solvents, bases and acids used in TSV fabrication
3. Have excellent adhesion properties to withstand the wafer thinning process
4. Maintain the global uniformity of 2 µm Total Thickness Variation (TTV) across the device wafer throughout the processing steps
5. Low temperature debonding which is compatible with solder bumps
6. Easy wafer clean process which is compatible with underlying layers of the device wafer

Due to the potential for widespread application of temporary bonding process several material solutions as well as equipments have been proposed and tested. For instance there are the thermoplastic materials based on Brewer Science, the polyimide based solution proposed by HD Micro, the BCB based solution proposed by Dow Chemical, the Light to Heat Conversion UV activated material solution by 3M, the perforated carrier support system by TOK, and the ZoneBond® solution proposed by Brewer Science. A more detailed account of the various technologies has been detailed elsewhere [6–10]. Though there have been multiple chemical solution as well as equipment modification as of today 3D IC integration is yet to become a mainstream technology. This we believe is due to the high cost associated with not just the material but the various steps in the temporary bonding and debonding process which affects the high throughput required for high volume manufacturing.

This paper is focused on a novel solution developed by Dow Corning Corporation which is a drop-in solution that does not require any special pre/post treatment of device or carrier wafers and is based on a simple spin-on solution.

Material Solution

Dow Corning Corporation (DCC) has developed a simple bilayer spin-on solution which has 2 Si-based materials which serve as the temporary bonding materials during the fabrication of thin wafers for 3D IC integration.

The bi-layer technology developed by DCC uses the following process flow

1. Spin coat thin release layer (RL) on device wafer and bake at low temperature (130 – 150°C)
2. Spin coat thick adhesive layer (AL) on either device or carrier wafer
3. Move both carrier and device wafer to bond chamber and complete room temperature bond without use of force or any heat
4. Cure bonded stack on hot plate
5. Wafer then goes through wafer thinning and TSV process
6. Laminate wafer pair on tape and debond wafer after post processing at room temperature

The above process flow was developed to simplify the temporary bonding/debonding process and reduce the cost associated with special equipment or processes for pretreatment and post treatment of wafers such as plasma, UV, preferential zone treatment etc. Additionally, the opportunity to process wafers at room temperature increases the throughput of the temporary bonding debonding process.

Figure 1 shows the process flow for the temporary bond/debond process using DCC’s temporary bonding material solution. The goal of each step in the temporary bonding debonding process flow is to maintain the device wafer TTV within 2 µm.

Figure 1: Process flow for DCC temporary bond/debond solution

Spin Coat Evaluation

The first step in the process flow is the spin coat evaluation of the temporary bonding materials. This is a critical step to avoid unwanted delay in process time, as the TTV of the spin coated material can add to the TTV of the bonded pair and later on transfer to the thin wafer during the wafer thinning and post processing of bonded wafer pairs. Thus it is important to start with a low TTV for spin coated films.

Since the temporary bonding material set developed by DCC is based on a bilayer technology we first evaluated the coating thickness and uniformity of the spin coated films on 200 mm blanket wafers before repeating the process on 300mm blanket wafers.

The Dow Corning® WL-3001 Bonding Release series which is a thin release layer coating was spin coated onto a 200 mm wafer and the thickness and uniformity of the coating was analyzed using the Filmetrics F-50 optical tool. The thickness of the spin coated film was found to vary from ~1300 Å to ~2800 Å based on the spin speed and the uniformity of the coating was <1%. Similarly, the spin coating evaluation of the Dow Corning® WL-40XX Adhesive series which is the thick AL was completed by spin coating the AL and measuring the thickness and the uniformity of the coated film to determine the baseline TTV that can be achieved using this material set. The coating thickness that can be achieved with the current AL material varies from 28 to 100µm based on the spin speed and the viscosity of the AL. The uniformity of the spin coated film was determined to be < 1% for a 66 µm coating thickness and the TTV of the spin coated film was 0.36 µm across the 200 mm wafer indicating that the spin coated films self planarize to provide a good starting point for achieving 2 µm TTV for the thin wafers. A similar trial was completed on 300 mm wafers to determine the TTV and uniformity of the AL. For a 68 µm coating the uniformity was
< 1% and for a 100 µm coating was < 2.5% with potential for further improvement via optimization. Figure 2 shows the spin coat evaluation of the WL-40XX series across a 200 mm wafer and Figure 3 on 300 mm wafer.

Figure 2: Spin coat evaluation of WL-40XX series AL on 200 mm wafer

Figure 3: Spin coat evaluation of WL-40XX series AL on 300 mm wafer

Bonding Experiments on 300 mm Wafers

The wafer bonding experiments were completed on the Suss Microtec XBS 300 Bond Cluster. A 300 mm blanket wafer was treated as the device wafer and the RL was coated on it. The wafer was baked at 130 – 150°C to drive out any residual solvent and cooled. The AL was then coated on top of the RL. The device and carrier wafers were then transferred to the bond chamber and aligned. The top wafer was then placed on top of the AL coated bottom wafer without the use of force or heating. This room temperature bond process greatly increases the throughput of the bond wafer without the use of force or heating. The bonded wafer pair was then transferred to the hot plate to complete the cure of the AL at 150°C. The TTV of the bonded pair was monitored after cure and for the current unoptimized bond process we were able to achieve a 4.1 µm TTV with 5 mm edge exclusion on a 68 µm thick adhesive coating. Figure 4 shows the wafer map of the thickness measurement across the 300 mm bonded wafer pair. The next step in our evaluation was to determine the robustness of the bonded pair by thinning down the blanket device wafer from 725 µm to 50 µm.

Wafer Thinning

The wafer thinning of bonded pairs were completed at DISCO US using the DGP8760. The bonded wafer pair went through a conventional 3 step backgrind process Z1 (coarse grind), Z2 (fine grind) and Z3 (polish). The process was repeated for all 8 bonded wafer pairs to see repeatability of the process as well as performance of the temporary bonding material. The blanket wafers were not edge trimmed and the wafer thinning process did not induce any edge chipping or cracking of the wafers. The TTV of the thinned wafer pair was measured using the Proforma 300 MTI Wafer Thickness Metrology optical tool. The TTV of the thinned bonded pair was found to vary from 2 – 6 µm. Figure 5 shows the picture of the backgrinded wafer whose final thickness is 50 µm. Figure 6 shows the wafer map of thin 300 mm wafer with a 2 µm TTV.

Figure 4: Wafer map of 300 mm bonded thick wafers with 68 µm AL coating

Figure 5: Photo of 50 µm thin non-edge trimmed wafer after backgrinding
Thermal Stability Analysis

The thermal stability of the temporary bonding materials is critical to ensure that the bonded stays bonded during the various processing steps involved in the via reveal and RDL fabrication steps. Additionally, it is important that the temporary bonding materials do not outgas during the post bond processing steps as it could lead to voids or delamination which in turn could lead to non-uniformity during the post bond processes which leads to failure of devices. Thus the thermal analysis comprises of two steps i) thermo gravimetric analysis (TGA) of RL and AL, ii) heat treatment of bonded pair and Scanning Acoustic Microscopy (SAM) analysis.

The TGA analysis of the RL and AL was completed by studying the weight loss of the cured RL and AL from room temperature to 300°C in air. This condition was used as this exposes the material to the harshest conditions for Si based materials. The weight loss for the RL as well as the AL was < 0.5 wt% from 25 to 300°C which indicates good thermal stability for the both the Dow Corning ® WL-3001 Bonding Release as well as the WL-40XX series.

The next step in the thermal analysis was to examine the thinned bonded pair for voids and/or delamination by heating the wafer pair to different temperature segments and time. The wafer thinned down to 50 μm was examined for voids after backgrinding using the SAM. The wafer pair was then placed on a hot plate at 200°C for 20 minutes in air and the SAM examination was repeated. No voids or delamination were detected. The same wafer pair was then exposed to 200°C for 3 hours and to simulate the solder bump reflow condition to 260°C for 10 minutes and analyzed using the SAM. No voids or delamination were detected using the SAM. As the final test 200°C, 3 hour heat treatment was repeated under vacuum condition of 45 Torr for 3 hours to examine if any voids develop due to the use of vacuum condition. The heat treated wafer pair was then reexamined using SAM and no voids or delamination were detected. This indicates that the temporary bonding material set developed by DCC can withstand not only the rigor of the backgrinding process but also meet the thermal stability required for withstanding the plasma processes such as PECVD etc. which are intrinsic to the fabrication of 3D IC’s. Figure 7 is the SAM images of the wafer pair exposed to various temperature conditions.

![Figure 6: 2 μm TTV across a 300 mm wafer pair thinned down to 50 μm thickness](image)

**Figure 6: 2 μm TTV across a 300 mm wafer pair thinned down to 50 μm thickness**

![Figure 7: SAM images of 50 μm thin bonded pair after thermal treatment](image)

**Figure 7: SAM images of 50 μm thin bonded pair after thermal treatment**

Chemical Resistance Analysis

The chemical resistance test is an important milestone for the temporary bonding process as the thinned wafer is expected to undergo several wet processes such as lithography, plating etc. where the temporary bonded wafer is required to withstand the chemicals without delaminating or swelling. The chemical resistance test was completed by spin coating an 8 inch wafer with the AL layer and curing it as per previously discussed conditions. The wafer was then soaked into different chemical compositions for predetermined time and the weight of the AL was monitored before and after soak to determine the weight loss or gain. The weight loss or gain was negligible for all chosen chemicals. Figure 8 shows the results of the chemical resistance analysis.

![Figure 8: Chemical resistance of AL to chemical used in 3D IC](image)

**Figure 8: Chemical resistance of AL to chemical used in 3D IC**
Debonding and Device Wafer Cleaning

One of the most critical steps to the adoption of the temporary bonding technology is the ability to debond the thinned device wafer from the carrier wafer and clean the device wafer from any residues. This is critical to ensure that the device wafer is not harmed and the yield seen in the Front End Of Line (FEOL) processes is maintained during the wafer thinning processes using temporary bonding technology.

As discussed in the background various material manufacturers have implemented different processes for debonding each with its pros and cons. For instance the traditional perforated carrier debond requires solvent soak. We have also seen the thermal slide off; Zone Bond and UV based debond solutions.

Our solution is based on the room temperature peel debond which is due to the engineering of the bi-layer technology. This was demonstrated using Suss Microtec’s DB300T and DB12T debonder. The debond evaluation was first completed on 300 mm thick wafers (725 µm). Once this was successfully completed then we repeated the process for 100 µm thin wafers and 50 µm thin wafers. The entire debond process is completed by first mounting the thinned wafer pair onto a dicing tape and placing it in the debonder. The thinned device wafer attached to the dicing tape is held in place on a vacuum chuck while the thick carrier wafer is peeled off. The entire debond process after the wafer mount in the debond chamber takes a couple of minutes. Then the device wafer which is attached to the dicing tape is cleaned using tape compatible solvent. Debond and wafer clean processes are completed in less than 5 minutes and based on our knowledge this is the fastest debond process available today. Additionally, during the debond process the AL is stuck to the carrier wafer whereas the solvent dissolvable RL is on the thin device wafer. This protects the device wafer from being exposed to harsh silicone removers or other strong acids, bases or a combination of heat and solvent treatment. Figure 9 shows the image of a 50 µm thin wafer after debond on a tape.

Figure 9: Shows the photo of a 50 µm thin wafer after debond on a tape

Bumped Wafer Evaluation

The final evaluation was to complete the coat, bond, wafer thinning and debond of bumped wafers. Bumped wafers with 45 micron tall bumps and 70 micron tall bumps purchased externally were used in the bumped wafer evaluation.

As the first step the height of the bumps were measured using a profilometer to compare the results with the data provided by the vendor. After confirmation of the bump height as the next step the bumped wafers were coated with DCC temporary bonding material sets of Dow Corning ® WL-3001 Bonding Release and WL-40XX series and bonded using the Suss XBS300 bond cluster. SAM images were completed to check for any thickness variation or voiding of the bonded pair. No voiding or thickness variation was seen for the bonded bumped wafer pairs. The bonded wafer pair was then thinned down to 50 µm by DISCO and the TTV of the thinned bonded wafer pair was examined as described previously. We were able to demonstrate a 2 µm TTV with a 5 mm edge exclusion on the bumped wafer with 45 µm tall bumps and 70 µm AL coating and a 3 µm TTV on the bumped wafer with 70 µm bumps and 100 µm AL coating after wafer thinning. The thinned wafers were then debonded using the Suss peel debonder and the device wafer was solvent cleaned. Figure 10 is the photo of the 50 µm thin debonded bumped wafer after wafer clean.

Figure 10: Photo of 50 µm thin debonded bumped wafers after peel debond and wafer clean

The results prove that the temporary bonding material set developed by DCC helps meet the 2-3 µm TTV requirement for tall bumps (45 – 70 µm) using our existing material set and allows for an easy debond and device wafer clean.

Conclusions

In this paper we completed the study of the novel temporary bonding material technology developed by DCC for thin wafer handling. We completed the material evaluation and demonstrated a total solution that provides < 1 µm TTV for 68 µm thick spin coated temporary bonding adhesive material. Additionally, we demonstrated the following performance and benefits based on our material solution

1. No pretreatment of wafers prior to coating or bonding.
2. Fast room temperature bond process which does not require the heating and cooling of bond chamber.
3. 2 & 3 µm TTV after backgrinding of thick wafers to 50 µm final thicknesses with 45 µm and 70 µm solder bumps.
4. Thermal resistance of bonding material with < 0.5 wt% weight change from room temperature to 300°C.
5. Void free thinned bonded pair verified by SAM imaging before and after thermal treatment at 200 °C for 3 hours and at solder reflow temperature.
6. Minimal weight change due to exposure to chemicals used in 3D IC post processes.
7. Room temperature debond and cleaning of device wafer.

Finally, the entire coat, bond, backgrind and debond process has been successfully demonstrated on bumped wafers.

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