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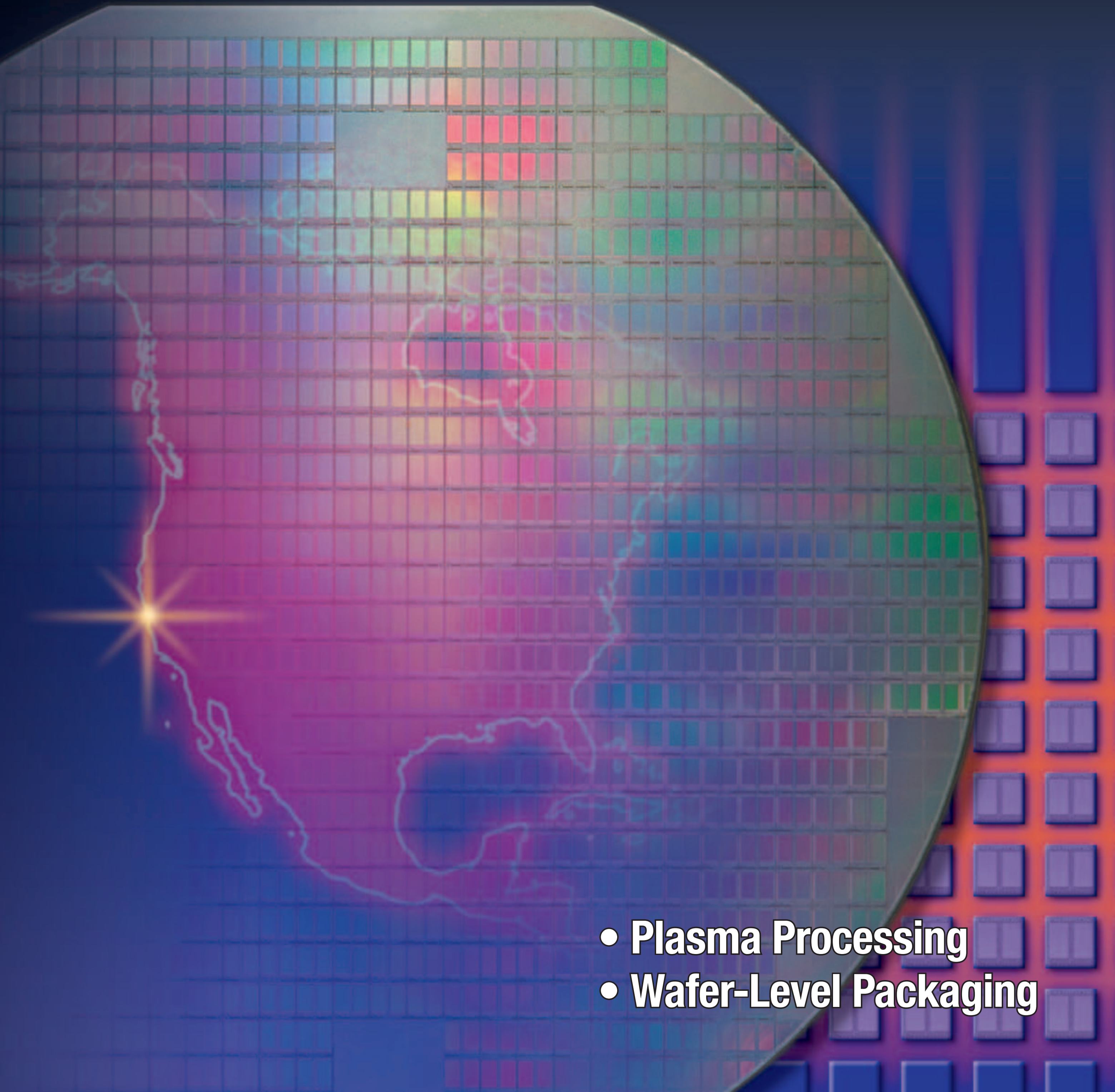

• Plasma Processing
• Wafer-Level Packaging

A New Approach to Wafer-Level Packaging Employs Spin-On and Printable Silicones

New material families that address today's wafer-level processing needs include photo-patternable spin-on and printable silicones that offer thermal stability and minimize stress. Employed in suitable applications, they offer enhanced productivity in manufacturing.

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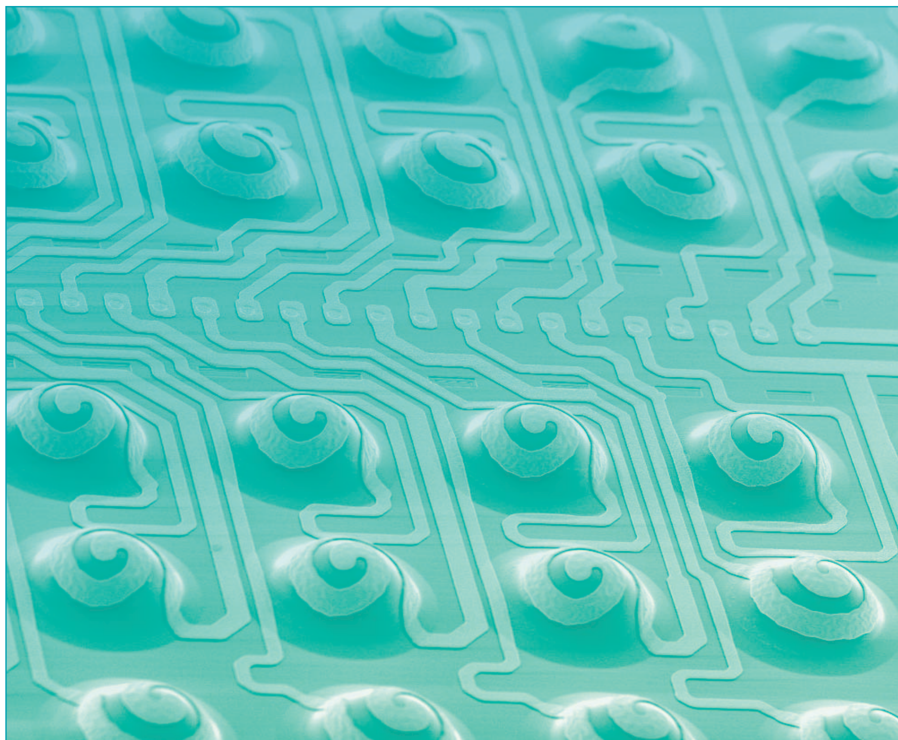

A 256Mb DRAM device packaged at the wafer-level using Cu/Ni/Au spiral metallization over printed silicone bumps. After singulation the devices can be assembled using conventional SMT equipment without an underfill.

The 2003 version of the International Technology Roadmap for Semiconductors (ITRS) views wafer-level packaging (WLP) as a promising solution for future packaging and interconnect challenges.

WLP offers the potential of lowering the overall cost of device packaging. It also promises to help keep packaging costs more stable in future production as die shrinks occur.*

The quest for cost control, and the need to increase device electrical performance through shorter interconnects, is contributing to the adoption and high growth of devices packaged at the wafer level. Indeed, Prismark Partners, a consulting firm, predicts a five-fold increase in WLCSP production from 2002 to 2007.

There are commonly four different WLP design concepts being evaluated and used in the industry. These designs range from encapsulated beam lead or wire-bonded structures to copper posts encapsulated with a resin system.

Redistribution Technology

The most prevalent designs, based on the high number of companies with WLP packages, are employing redistribution technology. This design refers to the redistribution of bond pads to other locations on the chip (sometimes onto a polymeric bump) by metalizing over a dielectric material.

Various materials, processes and methods exist for creating the redistribution and bump layers on a device. The subject of this article is the incorporation of elastomeric bumps into the wafer-level redistribution design—a process that has yielded improved reliability, simplified testing and ease of process compatibility with existing infrastructure.

Many readily available methods can be used to apply elastomeric bumps to substrates, but the two primary processes for creating such patterns on wafers are stencil printing and spin-coating/photolithography.

Spin Coating

A traditional spin-coating process begins by spinning a blanket film of solvent-based material onto a wafer, followed by a solvent vaporization step. The material is either directly patterned using photolithography (commonly a UV-light source and a mask or reticle), or it can be patterned with a photoresist.

The unwanted portion of the film is removed (developed) in a chemical solution and baked, typically in a controlled environment and at fairly high temperatures (usually 300-400°C).

This basic process is common to most integrated device manufacturers, since currently available materials all require the same general steps.

Expensive track coating and photolithography equipment, however, can be impractical for many packaging applications. More appropriate for many designs would be a simpler stencil printing process, where a material is patterned solely by printing through apertures in a stencil.

Stencil Printing

From a cost-of-ownership standpoint,

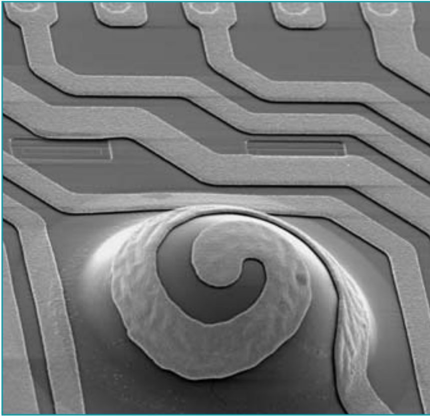

Figure 1. The redistribution layer is achieved by sputter and plate.

printing holds a significant advantage over spin-coating. The capital cost of printing equipment is a fraction of that for spin-coating or photolithography equipment, and printing offers significant throughput gains.

Printing allows much greater flexibility than current alternative processes, because new designs can easily be implemented by simply changing the stencil and print parameters. Compared to photolithography masks and reticles, these stencils are roughly an order of magnitude lower in cost. Additionally, the potential economic and environmental benefits of eliminating solvents and developing solutions employed in photolithography or spin-coating can be substantial.

Great technical strides have been made by suppliers to transform a conventional surface-mount technology printing system into equipment suitable for high-precision semiconductor packaging applications.

Improvements in stencil design, tighter control of alignment tolerances, new methods for handling wafers and carefully engineered rheology of printing materials are just a few of these advances.

Constraints

Despite its advantages, some constraints to stencil printing remain. The major limitation is that very fine pitch or extremely small feature sizes are still unattainable using stencils only. Feature size and pitch are determined by the ability to drill large numbers of small holes in a very dense pattern (or grow/fabricate them using electroplating) cost-effectively.

At some point, the holes become too small to print through or too dense to maintain stencil integrity, requiring the use of alternative processes.

Cost-sensitive devices with moderate-to-low density interconnect patterns, such as memory products, are viewed as ideal candidates for WLP, since the typical chip size and pincounts enable the use of standard, low-cost boards with pitches of 0.65mm and above. The transition to 300mm wafers more than doubles the number of chips per wafer, further reducing cost per die.

New Materials

Two recently developed material families promise to address today's wafer-level processing needs. The first, a series of photo-patternable spin-on silicones, is designed for optimized processing and reduced-temperature cure (150°C) in high-precision, small-pitch designs.

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The second, a series of printable silicone materials with tightly controlled rheology for use in conventional stencil printing operations, meets the needs of lower-density, high-volume applications. Both material sets are thermally stable and minimize stress.

The material that comprises the soft bump shown in Figure 1 is a fairly low-modulus silicone elastomer with a Young's modulus of 6.0 megapascals. The chemistry utilized offers advantages for WLP applications that include such as low-temperature cure, low moisture absorption, and the stability of physical and electrical properties over a wide range of temperatures and frequencies.

The rheological profile of the stencil-printable material has been optimized for creating soft bumps, including its viscosity, shear behavior, creep, recovery and other properties. Internal testing has shown that bumps ranging from 25µm to 175µm in height can be printed using a single-pass process and exhibit excellent co-planarity across the wafer. For taller heights, a two-pass process may be implemented to improve co-planarity.

Integration

The new printable materials are the result of a joint development project between Dow Corning and Infineon Technologies, initiated in 2000, which focused on developing new, more reliable memory products that could be produced more efficiently than existing processes allowed.

The scope of the effort was not restricted to packaging, but was committed to achieving critical flexibility in new materials, which could then be incorporated into a low-cost manufacturing operation that featured parallel testing at the wafer level to reduce process complexity.

The key elements of the new elastomeric bump technology are:

- Redistribution of pads to an area array in PC board pitch;
- Replacement of rigid solder balls by an elastic interconnect element;
- Backside and edge protection of the silicon die; and
- Ease of processing by only using solder during the final module assembly.

These features are achieved with a low complexity, mainly parallel process flow, with all bumps on the wafer applied in one step via stencil printing.

To produce packages of smaller height (down to 500µm), the target value for the new device architecture is a bump height of 170µm in the first step, which represents a height reduction of 50 percent compared to conventional interposer-based packages.

The small standoff easily allows bump pitch reduction down to 500µm or less, also an improvement over conventional solder bumped WLP (>300µm ball diameter). Another important advance in the elastomeric bump design is that underfills are not needed, due to the bump's flexibility.

The redistribution layer (Figure 1) of

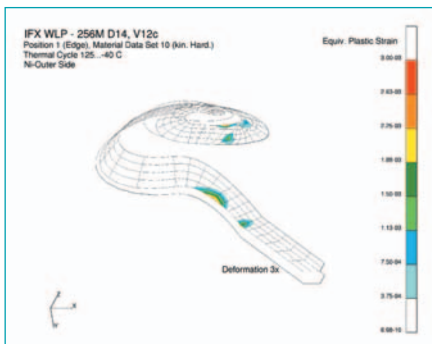

Figure 2. This finite element model shows spiral metallization.

the pads from the chip to the bumps is achieved by sputter and plate. The metal stack is applied after structuring a resist with photolithography. The metal stack is situated on top of the bump, making the electrical contact with the interconnect pads in test and assembly.

Spiral RDL

The plated metal is a Cu/Ni/Au stack, with a high conductivity due to the copper. In addition, because of the gold finish, The metal serves as a reliable pressure contact surface for test and burn-in and as a solderable interconnect pad in second-level assembly. The RDL was developed as a spring (or spiral) for increased contact reliability in testing and in service, a design which shows little inductance increase up to frequencies of approximately 1 GHz.

The spiral RDL contributes greatly to reliability and the accompanying finite elemental analysis model (Figure 2) shows the low stresses that result when the device is cooled from 125°C to -40°C.

As shown in Figure 3, the WLP build-up process steps are performed at or below 180°C, ensuring a minimal thermal load for the sensitive memory die.

This is an advantage that cannot be achieved with a solder ball-based interconnect element. During test and burn-in, the low complexity of the new technology is apparent: The elastic bump is contacted by a low pressure force (one to two grams per bump) on a flat contactor board.

Figure 4 shows the principle of the contact and the force-deflection behavior of the bumps. This arrangement is far less complex than the conventional contact by an array of pins.

Low-Contact Resistivity

Due to the Au/Au contact surfaces, this is a reliable contact with low resistivity without oxide layers that have to be pierced by the test equipment. The low-contact resistivity allows use at very high frequencies (up to 10 GHz) with high reliability (at a very low contact force), even when exposed to high temperatures (130°C) for as long as a week.

In module assembly, only the top of the elastic bump is soldered to the substrate. This is done in a conventional SMT line using standard solder paste print, pick and place for passives and DRAM packages and solder reflow (actives and passives). No special adaptation of the line is needed.

To obtain good thermal behavior of the package and to achieve high mechanical robustness, a heat spreader (HS) is implemented. The spreader can be realized in two different ways: at the module level over a full module side (as typically used, such as in Rambus modules) or just over a single package (a type of lid).

With a lid, the thermal behavior of the package can be improved over a conventional ball grid array (BGA). The R_θ value of this package is about 10K/W smaller than the value for a BGA (≥30K/W), which results in a lower junction temperature during service.

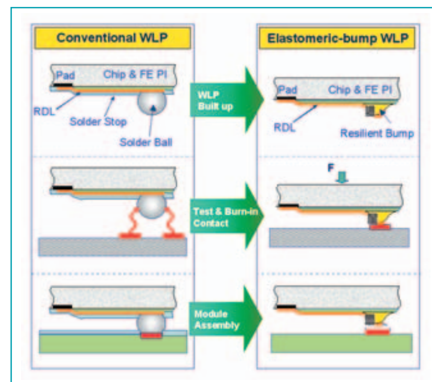

Figure 3. Elastomeric-bump WLP interconnect system compared to conventional WLP

test vehicles to investigate the interconnect reliability. (The table shows an overview of the tests.)

All tests at the component level and the module level showed excellent results, without any interconnect-related failures. One highlight of the tests was the reliability during temperature cycling: Even with a small bump height of 170µm, the test module easily reached 1000 temperature cycles (-40°C to 125°C).

In an ongoing test, a characteristic lifespan of >6500 cycles is predicted.

In addition to the accepted reliability tests, special tests adapted to the package (interconnect) were also performed, including outgassing, contact reliability, force deflection stability, shear properties and bump uniformity.

The material demonstrated comparable or superior performance to standard BGA packages in all areas. A critical issue was proving the mechanical stability of the package, and when assembled with a lid to simulate actual service, the package survived the mechanical shock test of 1500xg without failure.

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Reliability

Verification of first- and second-level reliability was conducted under Infineon Technologies' standard test conditions.

Interconnect-related reliability tests were used to evaluate the printable silicone, including a pressure cooker test, high-temperature storage and temperature cycling at the component level; as well as high-temperature storage and temperature cycling at the module level.

All tests were performed on daisy-chained

Conclusion

The development of new, printable silicone materials and elastomeric bump wafer-level packaging technology offers rich opportunities for enhanced produc-

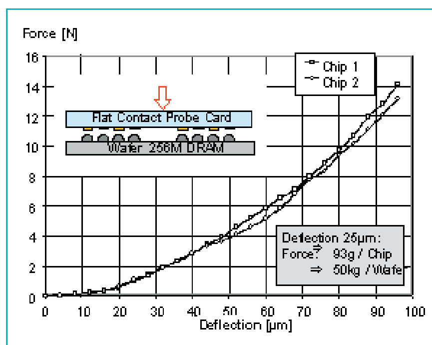


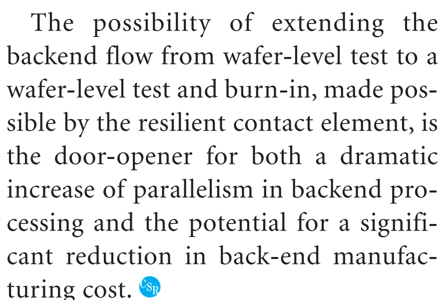
Figure 4. Force-deflection bump-behavior diagram

Component Level		
Test	**Condition**	**Result**
Preconditioning*	Shipping Simulation	Pass
Pressure Cooker Test	121°C, 2atm, 100%rh, 240h	Pass
High Temperature Storage	125°C, 1,000h	Pass
Temperature Cycling	-65°C/150°C, 1,000c	Pass
Thermal Humidity Test*	85°C, 85%rh, 1,000h	Pass
HAST (w/o Bias)*	125°C, 85%rh, 240h	Pass
Solderability*		Pass
ESD*		Pass
Module Level		
Test	**Condition**	**Result**
Temperature Cycling	-40°C/125°C, 1,000c	Pass
High Temperature Storage	125°C, 1,000h	Pass
Thermal Humidity Bias*	85°C, 85%rh, Vmax 500b	Pass
Application Test*		Pass
Pinch Test*		Pass
Bend Test*		Pass
Drop Test*		Pass
Vibration Test*		Pass

*=Tests done with comparable interconnect material

tivity in manufacturing, delivering excellent thermal, electrical and reliability performance along with the potential for the smallest form factors in packaging.

These properties can be reached by using the new resilient contact element combined with a thin-film redistribution layer. Due to the simple process flow and full parallel processing, this technology is now available at low cost.



The possibility of extending the backend flow from wafer-level test to a wafer-level test and burn-in, made possible by the resilient contact element, is the door-opener for both a dramatic increase of parallelism in backend processing and the potential for a significant reduction in back-end manufacturing cost.

* *International Technology Roadmap for Semiconductors (ITRS)*, Assembly and Packaging, 2003 Edition, page 17.

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